EMA Currents

Spring 2009

An Informative e-Newsletter from EMA Design Automation

Newsletter

New Release: Component Information Portal Version 2.2

In March, EMA Design Automation announced Component Information Portal™ (CIP) Version 2.2 - with over 5,000 components for CIP Enterprise and 1,000 for CIP, along with other usability enhancements. "Cadence® OrCAD® Capture CIS is a powerful tool for design capture and data

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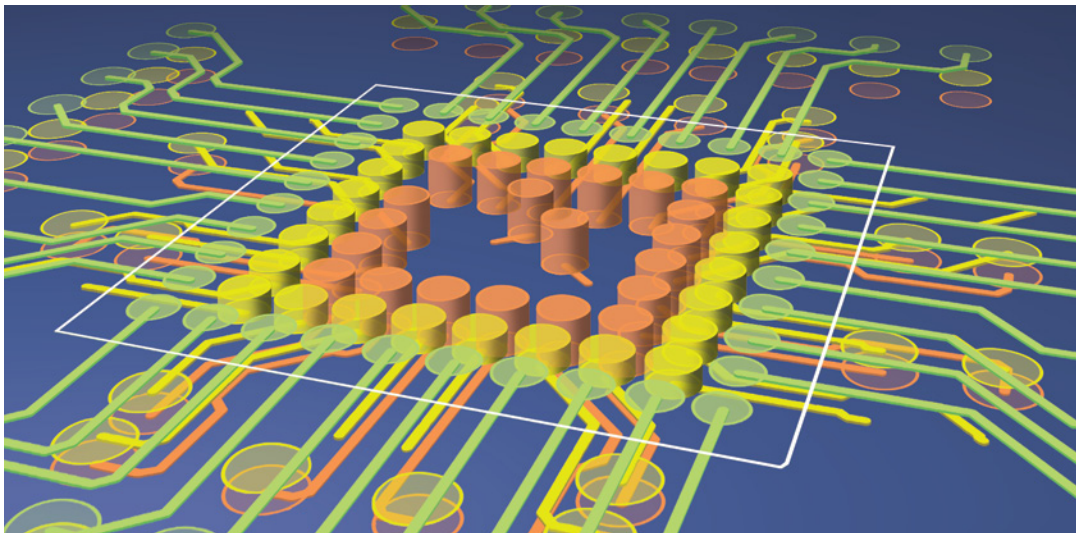
Also in this issue:



Implementing BGA Based Designs

By Helen Lebel
Application Engineer, EMA Design Automation

As BGA pin pitches continue to shrink, from 1.0mm to .8mm and below, designers must strategize how they will implement their projects. Designs that are driven by sub-millimeter BGAs demand specific methodologies and are usually classed as some of the toughest design challenges today, due to their physical layout constraints. When a decision is made to use sub-millimeter BGAs on a design, microvia technology may be chosen to complement the strategy. Advanced planning is essential to determine how the via strategy should behave during the route process. Neglecting the planning phase can cost precious time during the design and routing if the strategy was not given thorough consideration as to its accuracy.

One concern that can affect routing strategy is the type of methodology that will be used to produce the board. Common questions that need to be asked are: what type of manufacturing process will be used, such as will stacked or staggered vias be used, or is "via-in-pad" supported? How is the layer distribution planned and will it succeed given the rules and physical allowances? How will the power distribution be accomplished? Are there large areas which will demand power connections such as "dynamic shapes"? All these considerations can cut down on the available routing channels that need to be examined to ensure routing success. There are generally three categories used to examine a design before performing any routing. They are board criteria (including physical rules and electrical constraints), fanout routines and achieving successful breakouts, and finally overall routing strategies.

Board Criteria

While it is necessary to have rules and constraints, there are ways to manage them so they will not become barriers to routing. When dealing with

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Valor Acquires PCB Matrix

In January, Valor Computerized Systems, a global provider of productivity-enhancing software solutions for the electronics industry, acquired the assets of PCB Matrix Corporation, a leading provider of EDA library generation tools for both land pattern and schematic symbols.

PCB Matrix developed LP Wizard land pattern generation software as well as their recently released Symbol Wizard, which adds the automation of custom schematic symbol models using advanced component web search and links to deep, rich content.

Valor has built the world's largest geometric component database, known as the Valor Parts Library, with over 35 million parts for use in design and assembly applications, such as DFM, SMT Programming, and technical documentation. "We believe the industry will benefit from a streamlined library creation process that has the potential to incorporate manufacturing knowledge into the EDA libraries. This will ultimately lead to more manufacturable designs the first time through," says Patrick McGoff, VP Design Market at Valor.

Tom Hausherr, CEO of PCB Matrix, states, "It has been our vision for a long time to provide tools that eliminate the inefficiencies of CAD library generation. Joining forces with Valor, we now have the opportunity to take these applications to their full potential."

For sales and technical support contact EMA Design Automation, a reseller of Valor products.

Learn more about the Valor products we offer at: http://www.ema-eda.com/valor.

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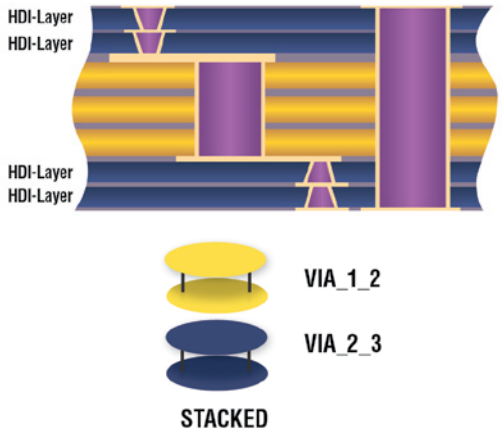
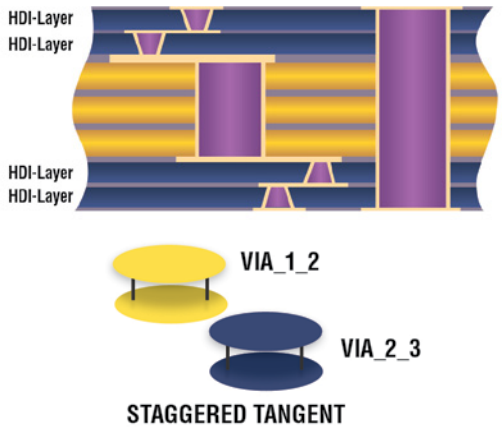
sub-millimeter pitch BGAs on a board,"region rules" can be used to control necking up or down in a BGA pin field area. This can help get route access to pads. Via types will certainly affect routing real estate, as shown in the illustrations. The type and size of vias for breakouts also will be a consideration for determining breakout and routing success. An illustration is included showing a stacked via configuration from layers 1-2 and then from layers 2-3. Because they are stacked, there "should" be more available routing channels on layer 2.



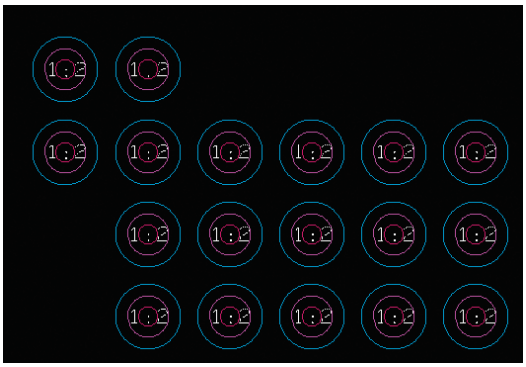
A second illustration is included to show a staggered via configuration from layers 1-2 and then layers 2-3. Rules can be set to allow for tangency if they are the same net.



Another consideration with constraints is verifying that physical constraints are not so complex that they will prevent routing success. A good rule of thumb with constraints is always use the lowest level of constraints necessary to get the job done accurately. Electrical constraints must also be verified, but these constraints are often inflexible. Examining all the rules and constraints can lead to a simplification of rule sets, producing a more elegant and simple set of rules that are accurate, but do not hinder the overall routing.

Fanout

It is vitally important to be sure that every pin used has a breakout to the appropriate layer on which it is intended to travel. "Via Labels" are great visual aids that assist in identifying pads when performing fanouts and other routing. Fanouts can be performed as a selective process in the Cadence Allegro PCB Editor application using **Route > Create Fanout** and choosing the Start and End Layers, the Via Type, the Via Direction, and finally the Symbol to apply the fanouts.

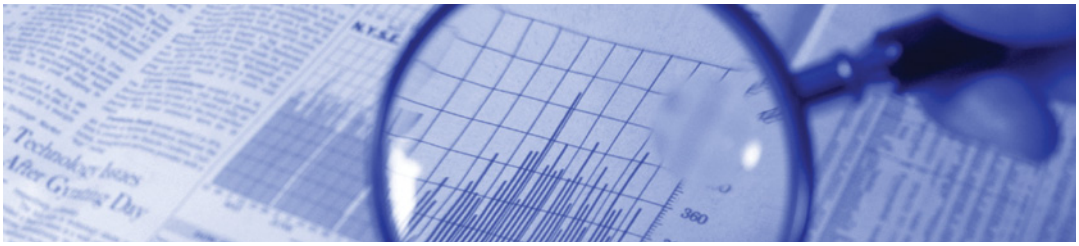


Fanouts also can be accomplished within Cadence SPECCTRA® for OrCAD using **Route > Pre route > Fanout**. Rules must be checked to be sure of the intended outcome. **Rules > PCB > General** has the setting to allow via-in-pad.

Route Strategy

With theses types of extreme boards, it is not uncommon to use a progressive routing strategy. This combines an interactive routing strategy with an automatic routing strategy. Designers pre-select certain nets to be routed, automatically route them, interactively adjust them to secure proper placement and cleanup, and duplicate these actions with other select groups of nets. Utilizing the power of the tools that exist within the user's license features can greatly assist a PCB designer in achieving route success.

Key elements of success to implementing and routing of tough, fine pitch BGA design are proper planning, understanding the full scope of requirements, and having enough confidence and skill to use the tools provided.



What's Up With Cadence?

By Bob Kelleher
Director of Sales, EMA Design Automation

Cadence Design Systems has been in financial news a number of times over the past few months. Several members of senior management "resigned" in October 2008. Cadence laid off 12 percent of their workforce in November 2008. Cadence's Q3 earnings call had to be postponed, and earnings from Q1 and Q2 had to be restated. In Q4, Cadence reported a loss of $1.46 billion, or $6.57 a share, a number largely inflated by a non-cash impairment charge of $1.36 billion. Cadence's earnings have been downgraded, and expectations have been lowered. With all this doom and gloom reported about Cadence lately, a lot of EMA customers have been asking, "What does this mean to me?"

In a nutshell, I would have to say "not much," unless of course you are an investor as well as a customer. I understand that as a customer you would like to see your supplier doing well financially. You have made an investment in purchasing these technologies, training your people on them, and setting up an infrastructure at your company to support their use. You are using Cadence technologies to design your electronics, and for many of you, that is an absolutely critical part of your business. So I understand if you feel a little uneasy at hearing all the bad news about Cadence.

> As a customer you would like to see your supplier doing well financially.

Most EMA customers are using the Cadence Allegro system interconnect design platform and/or Cadence OrCAD PCB design technologies, so let us take a good look at what the Cadence financial troubles mean to those products. The Allegro platform and OrCAD PCB design technologies are the primary products lines of the Cadence SPB division. SPB was hit very lightly by the November layoffs. Most of the SPB field sales and application engineering people are still there. Post-sales support and development are still intact too. Most of the people that were let go in November were from other product lines in other divisions.

The SPB division is still strong, but is Cadence in trouble of going under? I very much doubt that. Many of the problems Cadence faces stem from the fact they tried to grow by selling subscriptions too far out in time and discounting too deeply to entice their customers to spend 4 or 5 years of their EDA budgets upfront. So for a large percentage of their biggest customers, there is not much opportunity for more revenue for the next 2 or 3 years. Cadence needs to do a lot of belt-tightening for a couple years, but there are too many companies that rely on Cadence design technologies to let Cadence go under.

While it seems unlikely, what would happen to the Allegro and OrCAD product lines if Cadence does go under? Let us take a quick look at what happened to other EDA tools when their parent company went away. Scientific Calculations, Inc. developed a couple tools called SCICARDS and Encore BGA. Although Scientific Calculations no longer exists, both of those tools are still available (SCICARDS from Intercept and Encore from Sigrity). Cadnetix developed a PCB tool in the 80s, merged with Daisy in 1988 to become DAZIX, then filed for bankruptcy in 1990. The PCB tool went from DAZIX to Intergraph to Veribest, and is marketed today by Mentor Graphics under the name Expedition. In the worst case scenario, where Cadence goes out of business, the Allegro and OrCAD product lines would probably still be available and supported by some other company that acquires Cadence assets. The Allegro platform in particular has 35% market share in North America, making it the single most popular PCB product line. That sort of market share practically guarantees that, although Cadence could go away, the Allegro platform and its users would continue to be supported for the long term.

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Cadence eDA Card Basics

Cadence has two sales models for purchasing EDA tool licenses:

- 99-year license with annual maintenance
- Cadence eDA Card

The eDA Card is not a software license, but rather an account you can use to manage your license usage. The basic idea behind an eDA Card account is this: you put some money in an account; when you need a software license, you log into your account, download a time-based (temporary) license, and the license fee is deducted from your account.

Cadence eDA Card Advantages:

- Much lower price tag than a 99-year license
- Mix and match 99-year and temporary licenses
- Allows for WAN (Wide Area Network) licensing
- Try out new technologies without the large investment necessary for a 99-year license

In What Situations is the Cadence eDA Card Right for Me?

- If you have sporadic requirements for multiple licenses
- If you are unsure what licenses your company will need beyond this year
- If you are expecting your company to be sold or acquired in the next 5 years
- If you have a geographically diverse engineering team and would like to share licenses among them

With the exception of OrCAD PCB design technologies, most Cadence software is supported with the eDA Card. For more information, please contact your local salesperson.

First ISR for Cadence OrCAD 16.2 Available

Starting with the release of version 16.0, all software updates have been delivered as Interim Software Releases (ISR). This model for product updates continues with version 16.2. The first ISR for the OrCAD productivity tools is now available in the EMA Resource Center (ERC). There are 115 newly completed Product Change Requests (PCRs) in this update.

This update will be provided without charge to all current OrCAD customers with active maintenance contracts.

The OrCAD ISR is an incremental update which addresses critical software issues that could impact a user. It includes an installer which overlays the updated programs on top of a valid OrCAD 16.2 installation. The complete list of updates is posted in the ERC.

Future ISRs are planned to be released each quarter.

To gain access to the ERC, located at http://support.ema-eda.com, a username and password will be required. If you have not already registered with us, please visit the ERC and request your PIN number. Technical support is available by calling 585-334-6001 menu option 5.

Attention: Allegro platform users should download the Allegro Platform ISR in Sourcelink at: http://sourcelink.cadence.com.

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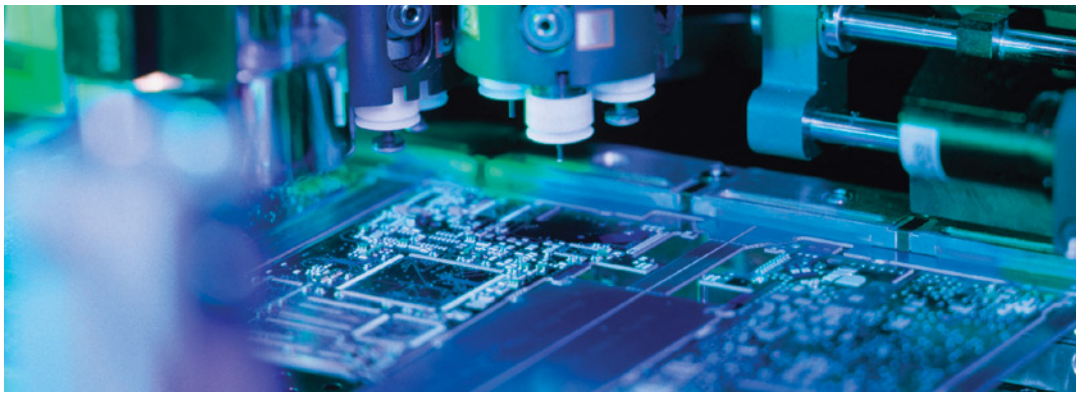
Times are tight all across the country, but it is good to see that Cadence is taking steps to ensure its long-term survival. While Cadence has made some mis-steps in the past, they have corrected many of the issues, learned from these mistakes, and are hardly in danger of going away. The Allegro platform and OrCAD PCB design technologies continue to be developed and remain an integral part of the Cadence future. The next release brings the promise of new innovations in how we use and interact with design software. So despite the negative press as of late, I am optimistic about the future of Cadence, and what that means for the customers we are proud to serve here at EMA. •



Design for Manufacture—The Great Enabler

By Paul Barrow
DFM Product Manager, Valor Computerized Systems, Inc.

"DFM"– a simple three character acronym that means so little, or so much, depending on your role in the design and manufacture process chain.

There are a number of forces driving the Design for Manufacturing process in today's electronics industry. Perhaps three of the most common are:

- The increase in component density due to new technologies
- The need for reduction on design cycle time
- The practice of outsourcing and off-shore manufacturing

The ever increasing need to make a design smaller and lighter, but with increased functionality, has resulted in new printed circuit board (PCB) fabrication technologies such as Sequential Build Up construction, designs featuring embedded passive and active components, and the introduction of component packaging technologies like Micro-BGA, Chip Scale Package, and Package on Package. This has made the design, fabrication, and assembly of PCB's a more complex task.

Reducing "time-to-market" is a critical requirement. With every PCB design iteration likely to add (on average) a couple weeks to the design cycle and lead to the late introduction of a product to the marketplace, it is imperative that manufacturability issues (one of the main causes of design iterations) are removed early in the PCB design phase.

To some, DFM is simply the running of some basic error checking on the PCB CAD system to determine that traces will not "short" when a PCB is fabricated or to ensure that components will not clash when a PCB is assembled. To others, it means the design has been optimized as much as possible to ensure the product can be fabricated, assembled, and tested in the most efficient way – with no special processes that incur additional costs in both time and money. A fully optimized design will even take into consideration the field failure rates of a product.

Let's take a step back and look at what companies are trying to achieve with a Design for Manufacture process when applied to PCB design.

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It is widely accepted that a product's design can have a significant and measurable effect on manufacturing process cycle times and unit production cost. In other words, a bad design takes longer to make and costs more! With the ever present pressures to reduce both costs and time-to-market, perhaps the best summary of why DFM should be implemented is to achieve cost effective manufacture. This is done by keeping yields high (i.e. less scrap) and minimizing the number of design iterations required. However, it also is important to recognize that applying DFM allows the full use of available process capabilities, such as state of the art technology – allowing (for example) a design to be implemented on one board instead of two, thus saving both time and cost.

DFM should not be used just to answer the question, "Can this design be made?", but rather, "Can this design be made effectively and therefore profitably?"

Most importantly, DFM must be thought of as a philosophy which permeates the entire New Product Introduction (NPI) process chain. It is not an afterthought or a "bolt on" extra which can be applied post-design. Yes, there are separate applications which can be identified as DFM tools. But in general, Design for Manufacture must be built into all the tools and should be "guaranteed" by the definition of the necessary rules up front and the enforcement of these rules throughout the tool chain. Many PCB design tools fit this model with a rules-based design philosophy the design tools either obey directly or at least are able to check against.

DFM must be thought of as a philosophy which permeates the entire process chain

Manufacturing (or production) needs to be split into its constituent parts. There are distinct and separate disciplines, namely Fabrication, Assembly and Test.

Fabrication covers everything concerned with producing the bare printed circuit board (including test/verification that it is free from defects).

Assembly deals with populating the bare board with the necessary components and also may include system level assembly (i.e. building a PCB into a system to form a complete product).

Test covers In-Circuit Testing (making sure the correct parts have been placed, are the right orientation, and have the correct values/operation) and Functional Test (validating the operation of the board as a whole to determine if it does what it was designed to do). The test discipline also tends to cover the issues of inspection and repair/rework.

Each discipline has its own specific requirements, and each area needs to be considered to ensure a good DFM result. It is no good just checking that a board can be fabricated if it then cannot be automatically assembled – especially if you must produce thousands (or hundreds of thousands) of assemblies.

Only checking that a design is free from manufacturing errors, however, is missing out on a major area which can have a significant impact on both the time and cost required to manufacture a design. In addition to checking the content of the design data against specifications or rules (feature sizes, clearances, spacings, etc.), it also is necessary to look at the number and type of processes required to produce the design. For instance, if the designer includes only one through hole device on the board, then he/she has immediately introduced at least one, and probably more (i.e. auto-insertion and wave solder), extra processes into the chain. This obviously makes a significant difference to the cost of each unit, and could be avoided by substituting an equivalent SMD component. Similarly, one 'odd-shaped' component that is not auto-insertable added to the design introduces the need for a manual placement station, which with more careful component selection could perhaps be avoided. In the fabrication field, going from a double sided board to a multi-layer one, or using blind/buried vias instead of through-board vias, adds yet more processes and potential sources of error, which also could be avoided.

There are two levels of DFM analysis. The first would involve simpler or "generic" tests (i.e. those common to all manufacturers and not affected by any single manufacturers' process capabilities). This category would include simple feature size and spacing checks, the use of two-dimensional placement shapes to guide component layout, etc. Although these factors can go some way to preventing manufacturing errors (assuming the rules are set up properly first), they do tend to produce a "worst case" result which does not give the designer enough help in making the best use of available technology and process capabilities.

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EMA Trade Shows

Design Automation Conference
San Francisco, CA – July 27-31
Visit EMA in Booth #3267
The Design Automation Conference (DAC) is the premier event for the design of electronic circuits and systems, and for EDA and silicon solutions. DAC features a wide array of technical presentations plus over 250 of the leading electronics design suppliers. Learn more about DAC 2009 at: http://www.dac.com/46th/index.aspx.

PCB West 2009
Santa Clara, CA – Sept. 15-16
Visit EMA in Booth #43-44
PCB West 2009 is an established annual conference and exhibition for PCB engineering, design, and fabrication professionals where you will have access to courses, technologies, solutions and contacts you can use to help grow your knowledge and your career. For more information visit http://www.pcbwest.com.

CDNLive! 2009
Santa Clara, CA – Oct. 1-2
CDNLive! 2009 offers a unique opportunity to network with industry experts and other power users of Cadence technologies. At this annual event, participants exchange ideas and best practices for boosting design productivity, eliminating risk, and developing differentiated products.
Learn more about CDNLive! at: http://www.cadence.com/cdnlive/na/2009/pages/default.aspx.

One-Day Tabletop Events

PCB Carolina 2009
Raleigh, NC – September 2
http://www.pcbcarolina.com/

EPTECH 2009
Quebec City, QC – Sept. 22
Halifax, NS – Sept. 24
http://www.ept.ca/eptech.asp

PCB Atlanta 2009
Atlanta, GA – October 22
http://www.pcbshows.com/atlanta/

NEW! 2009 Cadence Allegro Webinar Series

The Cadence Allegro Webinar Series highlights how the latest Allegro and OrCAD 16.2 technologies tackle current and emerging design challenges by providing new and enhanced capabilities to the end user. This free series incorporates many new and interesting topics.

Featured Webinars:

- Using Cadence PSpice Advanced Analysis for Complex Analog PCB Designs
- What's New in Cadence Allegro PCB Editor 16.2
- Accelerating Serial Link Compliance Testing
- Design Data Management for PCB Design
- PCB Library Creation
- Cadence Allegro PCB Editor Application Modes and Ease of Use
- What's New in IC Packaging/SiP

Have trouble attending webinars with your busy schedule? Not to worry, each of these webinars are archived for you to access at your convenience. For the complete list of archived webinars visit: http://www.ema-eda.com/training/webinarlanding.aspx.

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The second level DFM analysis requires a more detailed and accurate modeling of the processes required – the consideration (for example) of true component shapes and placement machine capability (component type handling, machine head/jaw geometry, and insertion sequence).

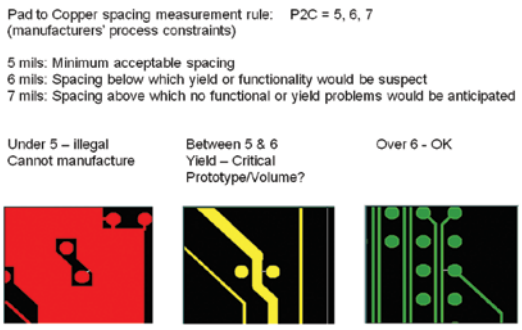
However, in order to get good second order results, there is the need to model the manufacturing processes to match the specific capabilities of the manufacturer who is going to produce the boards. The fabrication checks need to be done against the process capabilities of the chosen manufacturer; the assembly checks need to know which assembly machines are available and how they are set up. The facilities for test, inspection, and rework also need to be known. Achieving all this can be quite a problem, especially for those companies who do not do their own in-house manufacturing, as it is not easy to obtain this detailed process information from outside contract electronic manufacturers (CEM's).

Furthermore, not all aspects to be considered can be achieved by only referring to design data content. The setup of assembly machines (parts distribution to magazines), order of machines in the assembly line, balancing of the line to produce optimum throughput, etc., are all factors that need to be considered, and software tools are required for this. Although some people may consider this to be Production Planning, it all has a place in a good DFM process and demonstrates how important tasks, such as component selection and having a detailed knowledge of the assembly process set up, can help steer designers in the right direction to produce a design which can be manufactured efficiently.

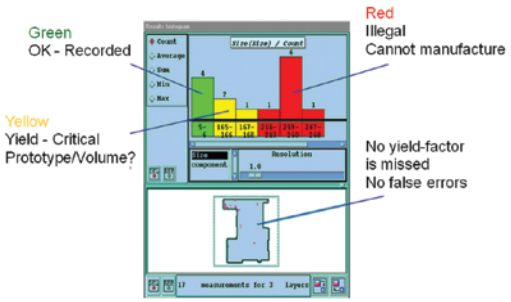
Because of the number and complexity of the rules, it is not possible for the PCB CAD tools to handle all of them, either automatically or interactively; especially if we take into consideration checks for heat dissipation, signal integrity, EMC, etc.

Therefore, it is necessary to concurrently use dedicated analysis tools to highlight potential problems, make suggestions as to how to fix them, and allow the user to trade-off the relative impact of each rule violation.

These specialist tools provide more than a basic "go/no-go" check, which is usually all a PCB CAD tool offers (see figure).



They can be configured to provide error severity ratings, giving the designer or NPI engineer more accurate information. This will enable more informed decisions to be made regarding what issues must be resolved (i.e. non-manufacturable), what issues should ideally be resolved (manufacturable under special approved conditions), and what issues can safely be ignored (no effect on manufacture/yield). With built-in calculators, various trade-offs can be applied.



Manufacturing: Not just a "go/no-go"

In conclusion, PCB Design for Manufacturing is the great enabler. It enables you to effectively increase the miniaturization of your designs without penalty, reduce the time-to-market of your products, and capitalize on global manufacturing trends with full confidence. Without it, your challenges are large, your costs are high, and your risks are immense. ●

Constraint Driven High Density Interconnect Printed Circuit Board Design Flow

By Hemant Shah
Product Marketing Director, Cadence Design Systems

Today's SPB 16.2 release is significant for the Allegro and OrCAD families of products, but more importantly, I think it brings a lot of new functionality for PCB designers.

First and foremost, we have added a constraint-driven PCB design flow for build-up designs to accelerate miniaturization.

As you know, customers in the high-end consumer electronics market place, mobile phone makers, and GPS navigation system makers have been dealing with miniaturization for quite some time and have been using build-up process to fabricate PCBs.

With smaller and smaller pin pitch BGAs being introduced, with 0.8 mm pin pitch or lower at 0.65, 0.5, 0.4 mm, there is no way to drill a through hole via through the BGAs.

While miniaturization is not necessarily the primary objective for customers in many other market segments (such as computing and networking), they are being forced to use build-up technology for fanning out a BGA — particularly if the BGA has 3 or 4 rows of pins on each side. For cost reasons, most customers tend to use two build-up layers on each side of the PCB and have the traditional rigid PCB as the core.

For customers in most (if not all) market segments, having a constraint-driven PCB design flow is a requirement. I have heard over the past 8-10 years the number of nets that have high-speed is growing.

With the migration to standards based interfaces, the number of constraints on nets is also increasing. Particularly with DDRx standard, there is not only an increase in the number of constraints on nets but there are a lot of additional constraints that are interdependent on each other.

For example, for DDR2 memories all data signals in a byte lane must be matched in length and delay. Clocks must be longer than the lengths of Address, Command and Control signals at the same time length of all the clock signals must be between the longest Data Strobe signal and the shortest Data Strobe signal.

When customers who are designing with DDRx are forced to move to build-up technology for BGA fanouts, they require a system that can handle both the design requirements coming from such standards based interfaces and also from the build-up technology using HDI.

Many Allegro PCB Editor users have been doing blind and buried vias for a while now with the constraint-driven flow. They have been asking us to enhance the capabilities to make it easier to design PCBs with HDI.

We really focused on this area to ensure our customers continue to get the benefit of our proven constraint-driven PCB design flow while working on HDI designs. It is not enough to do just HDI without a robust and comprehensive constraint-driven PCB design as a backbone.

Without the constraint-driven flow, customers may be able to create HDI designs faster only to find out later in the design cycle that the high-speed interfaces don't work.

This is just one of the new product enhancements available with the latest release from Cadence. For more information on SPB 16.2 visit: http://www.ema-eda.com/allegroHDI. •

On-Demand Demos

From beginners to advanced users, there are demos for every skill level ready to be viewed at: http://www.ema-eda.com/multimedia/.

Utilizing Relational Database Support in Cadence OrCAD Capture CIS

Starting in version 16.2, OrCAD Capture CIS allows you to create and use relational tables in your parts database. This presentation will show the benefits of using relational database support as well as how to view and search for relational data in OrCAD Capture CIS.

Accessing Digi-Key Part Data through Cadence OrCAD Capture CIS

The Component Information Portal (CIP) is the engine that drives the integration between OrCAD Capture CIS and Digi-Key®. This presentation demonstrates how easy it is to download Digi-Key part information directly into OrCAD Capture CIS. Viewers will discover how CIP's user friendly web interface can help automate new part requests.

PCB Matrix Symbol Wizard

PCB Matrix is revolutionizing the entire library automation process through the automation of schematic symbol models. This presentation demonstrates how to create a multi-part schematic symbol set and land pattern, based on a 1738-pin Xilinx BGA, in less than an hour using PCB Matrix Symbol Wizard.

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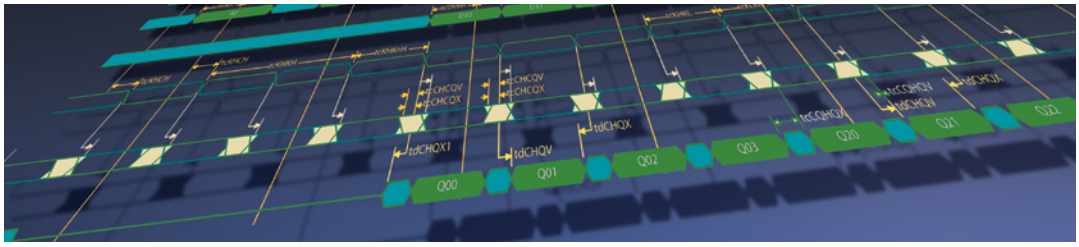
management," said Manny Marcano, president and CEO of EMA Design Automation. "Adding CIP and other EMA services ties it in to a corporate environment, and this new version will provide an excellent foundation for any organization trying to better manage and control their engineering data."

CIP Version 2.2 Features:

- 800 parts added to its existing foundation library, bringing the total to 1,000, and the CIP Enterprise foundation library now contains over 5,000 parts
- Utilizes the new relational database support in OrCAD Capture CIS 16.2. This provides new capabilities such as associating multiple manufacturers to a single part
- Advanced export feature allows users to update an external list of parts with information from the CIS database

CIP offers OrCAD Capture CIS users an impressive "off-the-shelf" CIS management environment. The CIP solution is ideal for engineering teams looking for a CIS database solution, as well as those that may not have a lot of experience working with databases like Microsoft Access and Microsoft SQL Server.

For more information on CIP visit: www.ema-eda.com/CIP.



Using TimingDesigner to Develop State Machine Architecture for Complex Interfaces

By Jerry Long – Application Engineer, EMA Design Automation
Sandy Helton – Principle Engineer, Xilinx Inc.

Introduction

TimingDesigner, from EMA Design Automation, has many powerful features that allow a multitude of timing and verification issues to be analyzed. Many companies employ TimingDesigner to aid in complex interface design and development, as it provides an easy, self-intuitive method to address static timing issues using timing diagrams. One such area is complex memory interface design and control. This paper presents some TimingDesigner "use model" ideas in common use today for development of Double-Data Rate (DDR) interface and controller design.

Designing controllers for DDR and/or Quad Data Rate™ (QDR™) memory devices presents some very unique timing challenges, such as signal skew analysis and adjustments, and specific clock generation and control, all to ensure proper clock/data relationships. Typically, DDR style controllers are implemented in FPGA devices due to their register-rich architectures, powerful PLL clock network generators, and memory interface friendly I/Os, all providing a highly efficient and flexible (i.e. programmable) environment to read, write, and process data. These memory interfaces are typically operating at frequencies of 200 MHz and higher, presenting non-trivial timing challenges.

However, the interface timing is not the only complex issue at hand. There also is the challenge of data management and manipulation within the FPGA fabric. Depending on the nature of the controller design at hand, the data preparation phase can be several magnitudes more complex than data capture. The complexity involves how to feed data processing units, most of which are completely independent from one another and can therefore be operating at different clock rates.

The unique features contained in TimingDesigner provide an environment for not only deciphering interface timing, but also allowing insight into data manipulation issues beyond the interface. Using TimingDesigner in conjunction with an industry standard HDL based simulator provides a methodology for functional verification and debugging of very complex design issues much faster than simulation environments alone. TimingDesigner can play a very prominent role in the identification and resolution of system operation and control issues, providing very high observability at a low-level of abstraction.

Memory Controller Design Challenges: State Machines

The advent of DDR style memory devices was necessary to overcome the bottle-neck in data processing paths: the access to the memory storage device itself. Data capture on both rising and falling clock edges of synchronous memory devices effectively doubles the data access rate and allows data processing engines the luxury of a more continuous data stream. As is usually the case when a substantial design challenge has been resolved, DDR memory opened the door to even more powerful controller applications with a voracious appetite for data. One very effective method for controlling these data processors is the use of synchronous state machines.

State machines are very powerful control mechanisms that can be designed with various configurations and styles, ranging from the very simple (a counter for example) to the very complex (a DDR memory controller and data processor). Due to the nature of complex state machines and their dependency on input signals as well as current state, they are easiest to implement with HDL conditional constructs such as IF-THEN-ELSE, and CASE statements.

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A topic of concern with state machine implementation is how the machine is encoded. The most common method of encoding a state machine is binary encoding where the total number of states can be encoded into a minimally sized bus structure (2N represents the total number of states and 'N' represents the encoded bus size). However, there is a trade off with binary-encoding in that the minimal amount of registers used typically require rather large decode logic equations for each next state event. Large decode logic translates to "wide" P-term equations which can consume quite a bit of timing latency.

One-hot encoded state machines use a single register for each state representation, and while this means there will be a higher number of registers in use, the encoding required for each is minimal. Minimal register encoding translates to "narrow" P-term equations for each state bit. Depending on the complexity of the machine and the number of states, the amount of registers required could quickly become quite large. But this is typically not a problem with the FPGAs of today, as their register counts are quite large. In addition, FPGAs have limited inputs to the configurable logic entity: usually a 4 to 6 input Look-Up Table (LUT). So one-hot encoding, with its smaller logic levels and higher register counts, is the most efficient, and therefore best suited, style of state machine implementation for FPGAs.

One-hot state machines do have some pitfalls to be aware of. Since each state is represented with just one bit active at any time, the collective bits that represent the state machine vector do not fully enumerate the states available, so care must be taken for recovery of illegal states (more than one state bit active at a time). The reset condition must be considered, as well as any next state decode latency that exceeds the clock period. All these issues are conditions that can cause the state machine to enter an undefined state and therefore must be tested for in the design process.

TimingDesigner as a State Machine Design & Analysis Aid

Powerful HDL Feature Set

TimingDesigner is an extremely versatile tool that provides designers with enough flexibility to implement static timing analysis for any digital interface protocol, experiment with various device configurations affecting timing performance, and provide incremental functional verification of design segments. With powerful features such as Verilog and VHDL compliant Derived Signals, Derived Clocks, and other patented processes, TimingDesigner provides users with the ability to prove out design ideas, verify existing design elements, and debug problem design areas very quickly.

TimingDesigner's Derived Signal and Derived Clock features provided a monumental step forward for one-hot state machine design tasks and the problems they present, especially since existing HDL design code can be used directly to emulate and model various state machine transitions and associated data path control operations. HDL support is key here since it is a common language for FPGA and ASIC designers, and therefore provides easy translation into TimingDesigner analysis tasks.

Validating State Machine Design

To describe how a state machine design can be monitored and validated, we will focus on the Verilog HDL language and concatenate the state bits into a TimingDesigner Derived Signal, creating a vector that provides continual status of current machine conditions. For a large group of one-hot state bits, this can be an incredibly complicated code statement to assemble, but TimingDesigner's ability to nest Derived Signals together allows designers to build the state bits up individually (or into several small groups) and concatenate them all together to present the information as a single vector. This is of tremendous value to designers.

In addition, the Value Decode option available for all TimingDesigner waveforms allows a unique mnemonic label to be assigned to each state for easy state identification within the diagram. These human readable vector names simplify state machine analysis and debug by reducing the effort level required to identify bit presentation for each valid machine state. Typically, as the complexity of the state machine increases, so does the number of states involved, and the more valuable this feature becomes.

TimingDesigner also provides the ability to hide waveforms and other diagram events. Each individual state vector can be hidden in lieu of the concatenated result, which makes for a very clean analysis environment and allows a sense of hierarchy so that designers are not overly concerned about the minute details that make up the state itself. This allows them to concentrate on the more important aspects of the machine operation such as state-to-state transitions.

For the complete whitepaper go to: http://www.ema-eda.com/TimingDesigner/StateMachine.

New Design Kits from Simtek Corporation

Simtek Corporation is the newest company to collaborate with EMA to provide timing models for TimingDesigner. The two companies have made available TimingDesigner Design Kits for the full line of industry leading Simtek non-volatile SRAMs.

"After realizing the value that is gained by using TimingDesigner in our own internal development environment, it was a natural progression to see the benefits Simtek customers can realize with TimingDesigner and interactive timing models of our devices. These models will help our customers meet their high-speed design challenges and allow them to design in our Simtek nvSRAMs quickly and with confidence," said Grant Hulse, Vice President of Worldwide Marketing at Simtek Corporation.

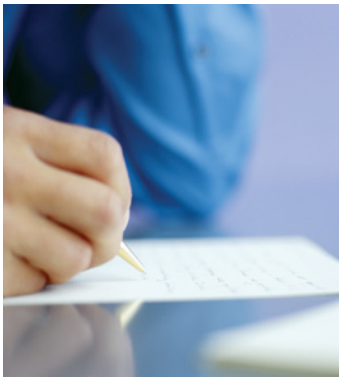
Simtek Corporation, headquartered in Colorado Springs, Colorado was recently acquired by Cypress Semiconductor and will now be a part of their Memory and Imaging Division.

The EMA TimingDesigner Design Kit Program provides pre-built timing models for popular devices and interfaces. Coupled with the powerful timing engine within TimingDesigner, users can quickly determine if design requirements will be met and perform what-if analysis to find optimum system performance.

The Simtek TimingDesigner models are available today for customers with active TimingDesigner maintenance contracts.

For a Full list of Design Kits visit: http://www.timingdesigner.com/Kitlist.

To learn more about Simtek visit: http://www.simtek.com.



Content Wanted

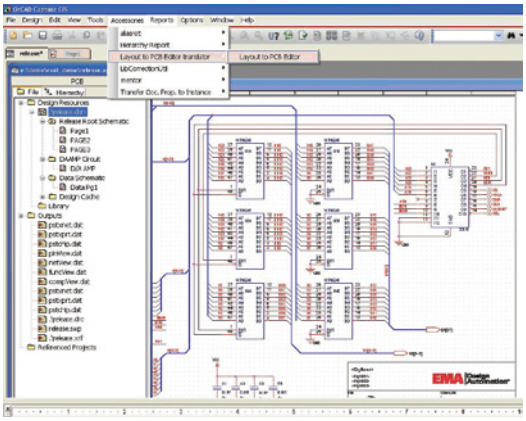
Have you ever wanted to share some of your experience with the engineering community? Have a topic you would really like to spout-off about? How would you like to get paid to do just that? Here is your chance to get your name in front of thousands of engineers. EMA is looking for technical writers to contribute articles for publication. We are looking for articles, technical tips, short tutorials, and white papers on current technologies and techniques centered on the Allegro platform and OrCAD PCB design technologies. If this sounds like something you would be interested in, please contact us at info@ema-eda.com for all the details.

Synchronizing Cadence OrCAD Capture and Cadence OrCAD PCB Editor

By Tim Ewell
Technical Support Specialist, EMA Design Automation

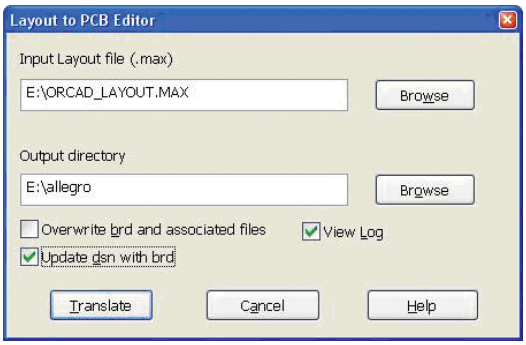
Cadence development has listened to your requests. The updated Cadence OrCAD Layout to Cadence OrCAD PCB Editor Translator, included in the recent Cadence SPB 16.2 release, now features synchronization of the Cadence OrCAD Capture schematic with OrCAD PCB Editor printed circuit boards translated from OrCAD Layout. Properties and footprint names are now back-annotated from the translated PCB into the original schematic, providing a ready-to-use design environment. Now that OrCAD Layout is no longer supported (as of March 31, 2009), this new function will become extremely valuable when moving designs into OrCAD PCB Editor.

The function of converting OrCAD Layout design files (.max) into OrCAD PCB Editor design files (.brd) is now located within the OrCAD Capture 16.2 accessories menu. PCB design databases created in any recent version of OrCAD Layout can easily be translated for use within OrCAD PCB Editor.



The OrCAD Layout to OrCAD PCB Editor Translator also lets you synchronize the OrCAD Capture design file (.dsn) and the OrCAD PCB Editor board file (.brd). During the translation process, the footprint names are changed to make them compatible with the Allegro platform.

If you select the "Update dsn with brd" option, the footprint names (PCB Footprint) are automatically synchronized with the OrCAD Capture design file. You also can specify the option "Overwrite brd and associated files" if you want to overwrite the existing files (such as the OrCAD Capture design file). It is always recommended to make a backup of your complete design prior to attempting any translation.



Many of our valued customers have taken advantage of technical demonstrations that assist users in migrating to the Allegro technology included in OrCAD PCB Editor. Three of the most popular sessions are:

Cadence OrCAD Capture to Cadence OrCAD PCB Editor – This introductory session is intended to familiarize customers with the OrCAD Capture to OrCAD PCB Editor design flow. It is highly recommended for users of OrCAD Layout interested in migrating to OrCAD PCB Editor.

Migrating Designs to Cadence OrCAD PCB Editor – When migrating to a new CAD tool, one of the primary concerns is to save important data in existing designs and libraries. This session demonstrates how to migrate data from other CAD tools into OrCAD PCB Editor. Customers will discover how to migrate library data and the steps needed to make it fully enhanced and compatible.

Cadence OrCAD PCB Editor Jumpstart – Based on Allegro platform technology, this jumpstart teaches customers the essentials for layout and routing using OrCAD PCB Editor. This jumpstart is designed for new users, OrCAD layout users transitioning to OrCAD PCB Editor, and frequent tech support callers.

Please call EMA technical support at 585-334-6001 opt 5 or send an email to techsupport@ema-eda.com to learn more about transitioning from OrCAD Layout to OrCAD PCB Editor. •

Selecting a Product Lifecycle Management Solution; The Needs of a Small Business

By Chuck Cimalore
Chief Technology Officer, Omnify Software

Quite often, a small or medium sized business (SMB) that is looking to gain a competitive advantage will do so by improving their products and streamlining their operations. Decision makers often look toward technology such as Product Lifecycle Management (PLM) to support these changes. By implementing a Product Lifecycle Management system, companies can simplify and shorten each phase of the product development process. Selecting new technology is a challenge for any organization, but can be especially difficult for the SMB since most software (particularly PLM software) is designed to meet the needs of a large enterprise.

To begin the selection process, the SMB first needs to understand what the PLM system should accomplish for its organization. PLM can provide key functionality to streamline each phase of a product's lifecycle, from product conception and design to manufacturing and support, while improving communication across both internal and external constituencies. A successful PLM implementation can help reduce time-to-market and decrease product costs, and also dramatically reduce waste and rework. Once a company determines that PLM software will address the challenges within their organization, the question now becomes which PLM software is best suited for their company.

Because the SMB operates with a smaller cash flow, develops fewer products, and has a smaller customer and supplier base compared to a large enterprise, the PLM system not only needs to address all development challenges, but it needs to be tailored to the distinct market segment. The increasing emphasis on outsourcing has dramatically changed the operational landscape of the SMB, and must be a key consideration when choosing the correct PLM system. Too often the SMB will select a PLM system that includes broad functionality, but fails to drill down into the daily challenges of engineers and developers to embrace the need to share product data outside the SMB's four walls.

PLM solutions designed for the large enterprise often manage few developmental logistics, and instead tout the capability to encompass supply chain management, packaging, and post-development phases. For the smaller business looking to improve products, the process should begin with the engineers who face issues with data management and communication with contract manufacturers and external partners.

A common misconception is that large PLM vendors with monolithic software systems are the only vendors that can address all product development needs. In reality, many of these large systems, which have been designed with large manufacturers such as automobile manufacturers in mind, include functionality that is irrelevant to the development needs of a small organization. Further, the SMB (with its limited cash flow) is paying for functionality that will likely never apply to its product design process.

Many smaller companies are beginning to look toward implementing PLM software designed for their market segment. In return, several large PLM and ERP vendors are attempting to "scale down" their products to address the PLM needs of the SMB. Unfortunately, because these systems are typically built on their legacy foundations, their heredity does not allow them to adapt easily to the evolving needs of the smaller organization. Moreover, these systems still require lengthy (and costly) implementation phases.

Implementation time and costs are critical factors for the SMB to consider when selecting a PLM system. SMBs cannot afford to reassign their valuable resources to long PLM implementation projects. Most software designed for the large enterprises have considerably lengthy implementation processes of more than six months. Alternatively, software designed for the SMB has a quicker implementation process and can have the company up and running within days or weeks, depending upon the vendor and level of integration with other systems.

SMBs often have a competitive advantage over their larger competitors when it comes to customer support and responsiveness. SMBs can react quicker to the evolving needs of their customers and target market, with intimate support and new

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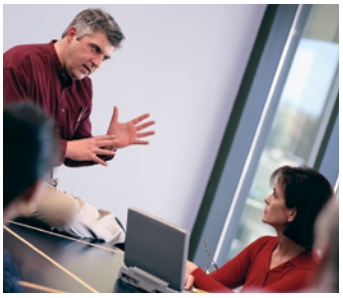
EMA Acquires DesignAdvance

In April, EMA announced its acquisition of DesignAdvance® and all of its intellectual property. "This acquisition builds on our EDA portfolio and strengthens our PCB solutions focus," said Manny Marcano, president and CEO of EMA. "This patented technology jointly developed by DesignAdvance and Carnegie Mellon University offers significant productivity enhancements for our PCB design customers."

As part of the acquisition, EMA has hired the key people responsible for creating and enhancing the DesignAdvance products, including Chandan Aladahalli, Ph.D., lead scientist and cofounder of DesignAdvance. This will allow EMA to continue the development of the three DesignAdvance products – CircuitSpace®, CircuitProbe™, and CircuitPlan™. "With EMA's deep penetration into the PCB design market, we'll be able to work with a broad range of customers to help solve their real world problems using our cutting edge technology," said Dr. Aladahalli. "EMA provides the customer interaction that allows us to tailor our aggressive roadmap and product development schedule to meet the specific needs of the marketplace."

CircuitSpace implements a hierarchical approach to PCB design through enhanced Autoclustering™ and replication technologies. CircuitProbe offers cross-probing between the Allegro PCB Editor or viewer and a PDF schematic. CircuitPlan provides planning, feasibility and design collaboration from concept level planning through physical design and test.

For more information about EMA and the products we offer, visit www.ema-eda.com.



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or enhanced products. This also should be an important consideration for the SMB when choosing a PLM system. SMBs should consider such purchases to be a "partnership" with the vendor. For the SMB, their PLM system needs to be easy to use, have a low total cost of ownership (TCO), and be from a vendor who is dedicated to the success of that SMB.

Finally, companies frequently overlook the importance of employee buy-in when selecting a new PLM application. If it is necessary for employees to learn an encyclopedia of information before using the software, the staff will be more resistant to using the tool and improving the product development process will be a greater challenge. In order to see a quicker return on investment (ROI), employees need a user-friendly PLM tool that requires limited ramp-up time. If employees feel comfortable using the software, they will be more likely to use it for a range of purposes. Within a smaller business, employees are expected to take on multiple functions, so it is likely they will need to understand many aspects of the software. If a software is easy to learn and easy to use on a daily basis, companies will see a greater and quicker transformation across the development process.

Selecting a PLM system can be a challenge if a company is not aware of the options available within the marketplace. But if an organization starts the process by understanding what the technology should address, and further understand the needs of their unique business and market segment, they can select a PLM tool that will allow the organization to develop products more efficiently and ultimately transform their organization.

Cadence Launches ActiveParts Portal

Cadence Design Systems

In November 2008, Cadence Design Systems, Inc. introduced its new ActiveParts Portal–an expansion of its Cadence ActiveParts online component data solution–that will offer PCB design teams even greater access to key component information. As part of the new ActiveParts Portal, Cadence is teaming with SupplyFrame, Inc. to provide engineers with new choices and even greater access to the component information they need to create their designs. In addition, Cadence announced new productivity-boosting technology and enhancements for the OrCAD Capture CIS and Cadence Allegro Design Entry CIS products.

Technology and enhancements introduced for the OrCAD Capture CIS and Allegro Design Entry CIS products include a new capability called Context-aware Non-Linear Graphic Editing. The capability is a new schematic editing technology for dense designs that provides a magnifying auto-zoom between focus points during editing operations. The latest OrCAD 16.2 release contains several other ease-of-use and productivity enhancements within the OrCAD Capture CIS and Cadence PSpice® A/D products.

The ActiveParts online database allows design engineers to find component information and directly incorporate symbols and data into the OrCAD Capture CIS and Allegro Design Entry CIS products. By collaborating with SupplyFrame as the first portal member, the ActiveParts Portal provides engineers with additional component information from a greater number of suppliers, significantly expanding the availability of component data and part information for engineers.

"Our goal is to help mutual customers make fast and accurate design decisions by providing critical information directly from the component manufacturer at the time it is needed," said Jeff Curie, Vice President of Marketing at SupplyFrame. "This collaboration delivers the latest symbols, datasheets, specs, and information on availability from thousands of manufacturers instantly from within the Cadence PCB design environment at no additional cost."

"Cadence is committed to developing the technology PCB designers need to do their jobs as efficiently and effectively as possible," said Josh Moore, Senior Product Marketing Manager at Cadence. "With the ActiveParts Portal and the additional new OrCAD technology, we've taken a big step forward."

OrCAD Capture boasts productivity and usability improvements, including an updated GUI and enhanced search capabilities, enabling users to work more efficiently and further shortening the design cycle. New FPGA design-in features include the ability to create split symbols, import and export FPGA pin assignments for leading FPGA vendors tools, and ease-of-use improvements for supporting the ECO process for FPGAs.